REMARKS

Reconsideration and allowance of the subject application in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-18 are pending.

Applicants note that during a telephone call with the Examiner held on May 30, 2007, the Examiner stated that the claimed system bus interface device was believed to correspond to bus controller 201 of Lin.

Claims 1-4, 9-14 and 16-18 are patentable over *Lin* (US Published Patent Application 2003/0046499) in view of *Ajanovic et al.* (US 5,859,988)

The rejection of claims 1-4, 9-14 and 16-18 under 35 USC 103(a) as being obvious over *Lin* in view of *Ajanovic* is hereby traversed.

At the outset, Applicants would like to kindly request the Patent and Trademark Office (PTO) to identify with specificity which elements of the reference are believed to correspond to the claim limitations. In the present Official Action (OA), the PTO appears to have referred to several different elements of the reference as corresponding to different claim limitations. For example, the PTO states that the interfaces 204A and 204C of the mass storage elements correspond to the first and second I/O bus interface devices without identifying which interfaces correspond to which claimed I/O bus interface device. Similarly, the PTO states that the local bus and PCI bus correspond to the first and second intermediate buses without identifying which buses correspond to which claimed intermediate buses.

Additionally, the PTO appears to assert that PCI interface 204C corresponds to the claimed first I/O bus interface device at page 2, section 4, line 11 of the OA and later asserts that local bus interface 204A corresponds to the claimed first I/O bus interface device at page 3, first line. Clarification is respectfully requested with respect to each of the elements of *Lin* asserted to correspond to claim limitations.

The PTO asserts that *Lin* discloses all limitations of claim 1, but admits that "*Lin* does not explicitly disclose a steering signal." Official Action mailed March 19, 2007 at page 3, line 6. The PTO assertion, at least with respect to *Lin* disclosing all remaining

limitations with respect to claim 1, is incorrect. There are at least four reasons *Lin* fails to disclose all remaining limitations of claim 1.

1. *Lin* fails to disclose a second intermediate bus as claimed

First, *Lin* fails to disclose a "second intermediate bus directly coupl[ing] the system bus interface device to the switching device" as claimed in claim 1. The PTO asserts that bus controller 201 of *Lin* corresponds to both the claimed system bus interface device and the claimed switching device. Further, the PTO asserts that the local bus of *Lin* corresponds to the claimed second intermediate bus.

The *Lin* local bus fails to meet the claim limitations as claimed in claim 1. The *Lin* local bus couples bus controller 201 and processor 100 local bus interface and couples the bus controller and local bus interface 204A. The *Lin* local bus fails to couple the asserted system bus interface device (i.e., bus controller 201) to the asserted switching device (i.e., bus controller 201).

Further, the PTO asserts that "Figure 2 illustrates the direct coupling of first I/O interface of 204a to first I/O bus interface 100." This assertion is not understood because the PTO does not appear to have mapped processor 100 to any of the claim elements. Assuming that the PTO is asserting that processor 100 corresponds to the claimed system bus interface device and the local bus corresponds to the claimed second intermediate bus, *Lin* still fails to disclose the claim limitation because the local bus interface 204A is not the claimed switching device. For at least this reason, withdrawal of the rejection is respectfully requested.

Further still, the PTO has already indicated that the *Lin* PCI bus corresponds to the claimed first intermediate bus and that PCI bus interface 204C corresponds to the claimed first I/O bus interface device. OA at page 2, section 4, lines 5-10. Therefore, as best understood by Applicants, the *Lin* PCI bus fails to couple the bus controller 201 to the bus controller as claimed in claim 1. For at least this reason, withdrawal of the rejection is respectfully requested.

2. *Lin* fails to disclose a switching device as claimed

Second, *Lin* fails to disclose a "switching device . . . operable to couple the second intermediate bus either to the first or to the second I/O bus interface device responsive to the steering signal" as claimed in claim 1. The PTO asserts that bus control 201 provides the claimed capability, however, this is incorrect.

Bus control 201 fails to couple the second intermediate bus (asserted to be the *Lin* local bus by the PTO) to the first I/O bus interface device or the second I/O bus interface device. Specifically, the *Lin* local bus appears to be coupled to local bus interface 204A regardless of bus control 201 operation. For at least this reason, withdrawal of the rejection is respectfully requested.

Further, as admitted by the PTO, bus control 201 fails to couple the second intermediate bus responsive to the steering signal.

3. *Ajanovic* fails to disclose a steering signal as claimed

Third, *Ajanovic* fails to disclose a steering signal to which the switching device is responsive, nor does *Ajanovic* appear to disclose a switching device operable to couple the second intermediate bus either to the first or to the second I/O bus interface device responsive to the steering signal as claimed in claim 1.

The PTO asserts that *Ajanovic* describes a steering signal to which a switching device is responsive. This is incorrect. The PTO-identified portion of Ajanovic, reproduced herein for ease of reference, states:

> Similarly, port C, comprising master/target interface 303, is coupled to the other secondary PCI bus 207. Port A 301 is coupled to port A/B data buffers 304 which is in turn coupled to port B 302. Port B 302 is coupled to port B/C data buffers 305 which is in turn coupled to port C 303. Port C 303 is coupled to port A/C data buffers 306 which is in turn coupled to port A 301. In addition, port A 301, port B 302, and port C 303 are each coupled to port B/C arbitration and control unit 308.
>
> *Ajanovic* at column 5, line 65-column 6, line 3.

The above portion of *Ajanovic* fails to describe a steering signal nor a steering signal to which a switching device is responsive. The above portion of *Ajanovic*

appears to describe the coupling of ports A, B, and C to port B/C arbitration and control unit 308 without describing a steering signal or a switching device operable responsive to the steering signal. For at least this reason, withdrawal of the rejection is respectfully requested.

4. No prima facie case of obviousness

Fourth, the PTO has failed to set forth a prima facie case of obviousness with respect to the combination of *Lin* with Ajanovic. Specifically, the PTO has failed to identify why a person of ordinary skill would be motivated to combine the *Ajanovic* bridge in the drive controller of Lin. "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F. 3d 977, 988 (CA Fed. 2006). The PTO has failed to articulate a reasoning supporting the applied combination of references and therefore the applied combination of references is improper. *Lin* appears to already contemplate adding additional devices to a PCI system bus, see e.g., paragraph 49. For at least this reason, withdrawal of the rejection is respectfully requested.

Further, the PTO reference to *Lin* at column 2, lines 50-58 is not understood because *Lin* comprises only pages and paragraphs. Further still, column 2, lines 50-58 (read as page 1, last portion of paragraph 11 through the first portion of paragraph 12) fails to identify the asserted motivation relied on by the PTO. Further still, column 2, lines 50-58 of *Ajanovic* fails to describe the asserted motivation, as well. For at least this reason, withdrawal of the rejection is respectfully requested.

Based on each of the foregoing reasons, claim 1 is patentable over Lin, singly or in combination with Ajanovic, and the rejection is respectfully requested to be withdrawn.

Claims 2-4 and 9-10 depend, either directly or indirectly, from claim 1, include further limitations, and are patentable over *Lin* in view of *Ajanovic* for at least the reasons advanced above with respect to claim 1. The rejection of claims 2-4 and 9-10 should be withdrawn.

Claim 11 is patentable over Lin, singly or in combination with Ajanovic, for at least reasons similar to those advanced above with respect to claim 1 and the rejection should be withdrawn.

Further, claim 11 recites a coupling of I/O bandwidth between: first I/O bus interface device and the system bus interface device, switching device and the system bus interface device, and second intermediate bus and either of the first or second I/O bus interface devices which are not found in the applied combination of references. For at least this additional reason, withdrawal of the rejection is respectfully requested.

Claims 12-14 depend, either directly or indirectly, from claim 11, include further limitations, and are patentable over *Lin* in view of *Ajanovic* for at least the reasons advanced above with respect to claim 11. The rejection of claims 12-14 should be withdrawn.

Claim 16 is patentable over Lin, singly or in combination with Ajanovic, for at least reasons similar to those advanced above with respect to claim 1 and the rejection should be withdrawn.

Claims 17-18 depend, either directly or indirectly, from claim 11, include further limitations, and are patentable over *Lin* in view of *Ajanovic* for at least the reasons advanced above with respect to claim 11. The rejection of claims 17-18 should be withdrawn.

Claims 5-8 and 15 are patentable over *Ajanovic et al.* in view of *Alexander et al.*

The rejection of claims 5-8 under 35 USC 103(a) as being unpatentable over *Ajanovic* in view of *Alexander et al.* (US Patent 6,510,529) is believed overcome in view of the foregoing arguments with respect to claims 1 and 11. Claims 5-8 and 15 depend, either directly or indirectly, from claims 1 and 11, include further limitations, and are patentable over *Ajanovic* in view of *Alexander* for at least the reasons advanced above with respect to claims 1 and 11. Withdrawal of the rejection is respectfully requested.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application should be in condition for allowance and a Notice to that effect is earnestly solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025 and please credit any excess fees to such deposit account.

Respectfully submitted,

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